# On the Crack and Delamination Risk Optimization of a Si-Interposer for LED Packaging

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**Abstract**

3D-integration becomes more and more an important issue for advanced LED packaging solutions as it is a great challenge for the thermo-mechanical reliability to remove heat from LEDs to the environment by heat spreading or specialized cooling technologies. Thermal copper-TSVs provide an elegant solution to effectively transfer heat from LED to the heat spreading structures on the backside of a substrate. But, the use of copper-TSVs generates also novel challenges for reliability as well as also for reliability analysis and prediction, i.e. to manage multiple failure modes acting combined - interface delamination, cracking and fatigue, in particular. In this case, the thermal expansion mismatch between copper and silicon yields to risky stress situations.

Therefore, the authors performed extensive simulative work to overcome cracking and delamination risks in the vicinity of thermal copper-TSVs by means of fracture mechanics approaches. Especially, an interaction integral approach is utilized within a simulative DoE and X-FEM is used to help clarifying crack propagation paths in silicon. The DoE-based response surface methodology provided a good insight into the role of model parameters for further optimizations of the intended thermal TSV-approaches in LED packaging applications.

## 1. Introduction

As a result of the ongoing progress in the development of smart lighting applications 3D-integration becomes also an important issue - advanced LED packaging solutions, in particular. To remove heat from LEDs to the environment by heat spreading or specialized cooling technologies is a great challenge for the thermo-mechanical reliability in this context. Thermal copper-TSVs provide an elegant solution to effectively transfer heat from LED to the heat spreading structures on the backside of a substrate. But, the use of copper-TSVs generates also novel challenges for reliability as well as for reliability analysis and prediction, i.e. to manage multiple failure modes acting combined - interface delamination, cracking and fatigue. In this case, the huge thermal expansion mismatch between copper and silicon yields to risky stress situations. Furthermore, out of plane pumping and protrusion of copper is a challenge for the metal- and dielectric layers covering the TSV during manufacturing (reflow soldering) and also during passive and active thermal cycling tests. First investigations demonstrate that these effects depend highly on the temperature dependent elastic-plastic behavior of TSV-copper and the residual stresses determined by the electro deposition chemistry as well as on the annealing conditions.

Therefore, the authors developed combined simulative/experimental methodologies to overcome cracking and delamination risks in the vicinity of the thermal copper-TSVs by means of fracture mechanics approaches. Especially, an interaction integral approach is utilized within a simulative DoE and X-FEM is used to help clarifying crack propagation paths in silicon. The DoE-based response surface methodology provided a good insight into the role of model parameters for further optimizations of the intended thermal TSV-approaches in LED packaging applications.

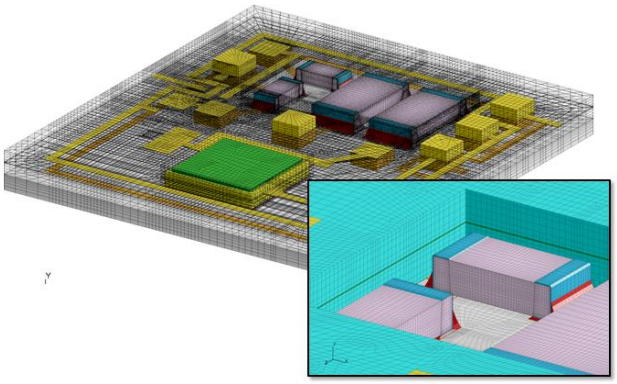


Fig. 1 2D/3D Wafer Level integration of a power module

Material properties as well as residual stresses taken into account for these simulations base on results of similar investigations regarding Cu-TSVs for microprocessor-memory 3D-integration explained in [1] and [2]. In this context a FIB trench technique combined with digital image correlation was used to capture the residual stress state near the surface of the TSVs. EBSD (Electron Backscattering Diffraction) had been realized at cross sections of several TSVs just to make the structural changes in TSV-copper clearer. Last but not least, nanoIndentation and a bi-material thermal testing approach helped to capture the temperature dependent mechanical properties of the TSV-copper utilized – see [3].

## 2. Delamination Risk near TSV

Different concepts of assembly and geometry approaches combined with different materials and boundary conditions were investigated in a design of experiments (DoE). It turned out that an increasing number of copper-TSVs decreases the temperature-differences by about 0.8 K. Moreover, of both initial crack vs. TSV diameter heat flux through the substrate as only few greater TSVs.

Apart from thermal management point of view thermo-mechanical issues have to be taken into account - the handling of the package in particular. For example, the thermo-mechanical loading of the silicon-carrier during the solder reflow and cooling down is of great interest in view of delaminations and damaging of metal and dielectric layers adjacent to the copper-TSV. Fig. 2 shows details of the TSV-vicinity of the simulation model. Especially the material interfaces near the TSV – marked by ellipses – between copper and the thin $SiO_2$-layer as well as between copper and nickel seem to be sensitive to delamination. The FE-model is fully parameterized. The constitutive behavior taken into account for all materials is explained in table 1.

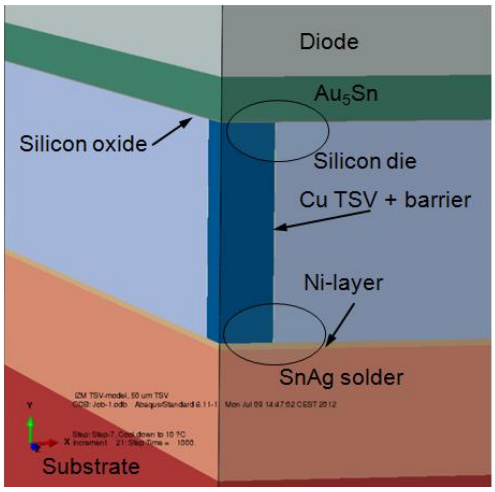



Fig. 2 Detail of the design of the LED-Package in the surrounding of a Copper-TSV

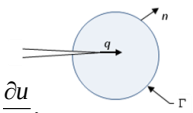
Table 1 Material constitutive behavior

| Material | Behavior |
|---|---|
| **Diode (germanium)** | Elastic |
| **Silicon** | Elastic (anisotropic) |
| **Copper** | Temp.-dep. elastic plastic, von Mises kinematic hardening |
| **Nickel** | Temp.-dep. elastic plastic, von Mises kinematic hardening |
| **SnAg solder** | Temp.-dep. elastic viscoplastic (creep) |
| **Ceramics** | Elastic |
| **Silicon oxide** | Elastic |
| **Barrier** | Elastic |

It is to be noted that the temperature dependent elastic plastic kinematic hardening behavior of TSV-copper is taken from investigations in [1]. The investigation of the delamination risk during the thermal handling is performed based with the J-integral as implemented in the commercial FE-code ABAQUS [5]. It can be expressed as

$$J_{\text{int}}^{\infty} = \lim_{\Gamma \to 0} \int_{\Gamma} n \cdot M^{\alpha} \cdot q \, d\Gamma$$

$$M^{\alpha} = \sigma : \varepsilon_{aux}^{\alpha} I - \sigma \cdot \left( \frac{\partial u}{\partial x} \right)_{aux}^{\alpha} - \sigma_{aux}^{\alpha} \cdot \frac{\partial u}{\partial x}, \qquad (1)$$




where $\Gamma$ is an arbitrary contour surrounding the crack tip, $q$ is a unit vector in the virtual crack extension direction, $n$ is the outward normal on $\Gamma$, $\sigma$ is the stress tensor and $u$ is the displacement vector. The subscription *aux* stands for the auxillary pure Modes I, II, and III crack tip fields for $\alpha = I,II,III$, correspondingly. It is implemented in the finite element code as a domain integral instead of the contour integral shown here and allows additionally the extraction of stress intensity factors by the use of the so-called pre-logarithmic energy factor matrix $\boldsymbol{B}$ [3]

$$J_{\text{int}}^{\alpha} = \int_{A} \lambda(s) n \cdot M^{\alpha} q \, dA \quad \text{and} \quad \mathbf{K} = 4\pi \mathbf{B} \cdot J_{\text{int}}, \qquad (2)$$

with $dA$ as a surface element on a vanishingly small tubular surface enclosing the crack tip. Note, that this K relates to the definition of the stress intensity factor introduced by Rice [4].

For this purpose initial delaminations have been introduced as shown in Fig. 3.

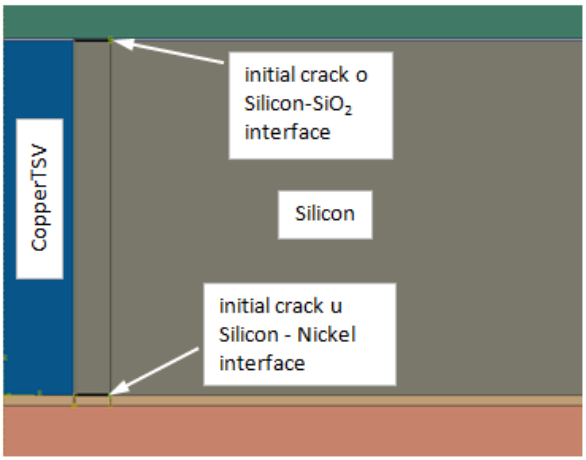



Fig. 3 Assumed initial delaminations at bi-material interfaces

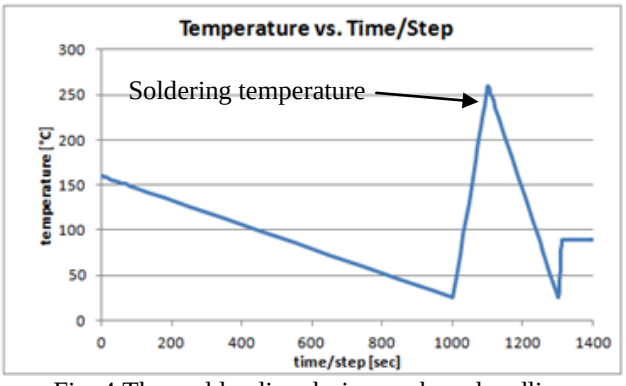



Fig. 4 Thermal loading during package handling

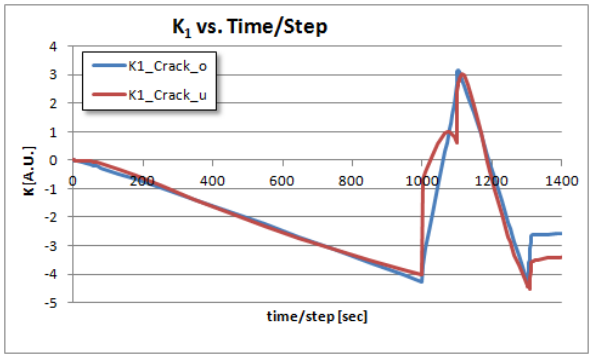



Fig. 5 $K_1$- progress of both material initial cracks during thermal loading - see Fig. 4

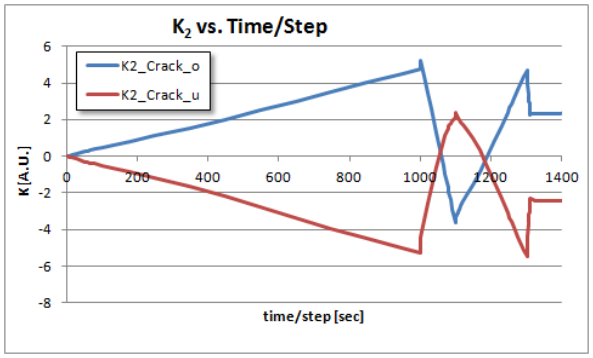



Fig. 6 $K_2$-progress of both material initial cracks progress during thermal loading – see Fig. 4

The stress intensity factors as to see in Fig. 5 and Fig. 6 result from contact behavior of the crack flanks during 1st cooling down to RT – that's why, we have a negative $K_1$. The highest value is achieved at the soldering temperature because of the relatively low initial stress free temperature and the CTE-mismatch driven expansion/ pumping at high temperatures. Whilst $K_2$ of both crack tips comes out with an opposite algebraic sign, $K_1$ of both crack tips seem very similar to each other. A phase angle of roughly 45 ° is to be noted at all times which means that frictional contact at the crack flanks had to be prepared which is the case for all simulations discussed here.

### 3. Delamination Risk Sensitivity to Geometry

The peak values of $K_1$ and $K_2$ are later on investigated via RSM (Response Surface Method) within a DoE exercise to clarify the sensitivity against changes of the TSV diameter, chip thickness and several layer thickness values, the thickness of the Nickel layer, in particular – see Fig. 2.

It can be seen that the SIFs of the upper interface delamination are widely independent of the thickness of the Nickel layer – crystal clear, why it is far away from the Nickel layer. With enhancing thickness of Nickel $K_1$ and also interaction integral $J_{int}$ decrease while $K_2$ increases – see Fig. 7 and Fig. 8. This means that the stress situation at the crack tip turns to a dominating shear mode. This is characterized by phase angles between 77° and 89°.

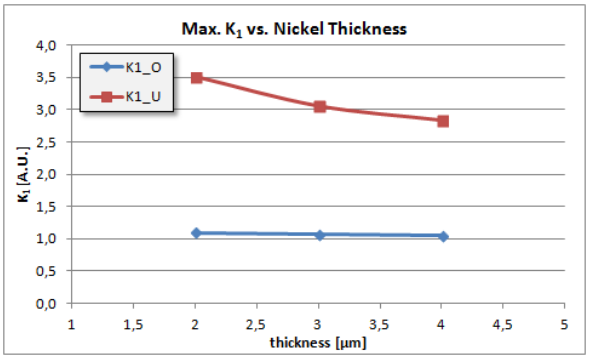



Fig. 7 $K_1$- progress of both material initial cracks vs. thickness of the Nickel layer

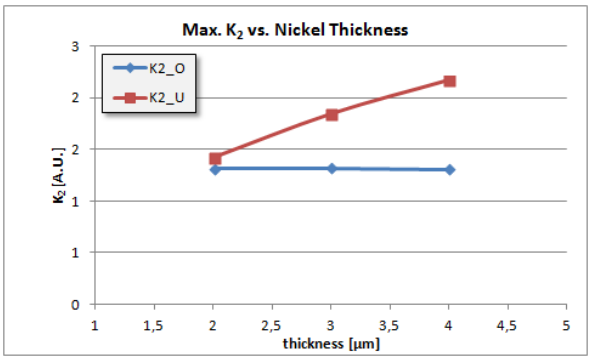



Fig. 8 $K_2$-progress of both initial cracks vs. thickness of the Nickel layer

Additionally, the influence of the TSV diameter is of great interest to follow or not the rules found by thermal simulations: multiple tiny TSVs show better thermal performance.

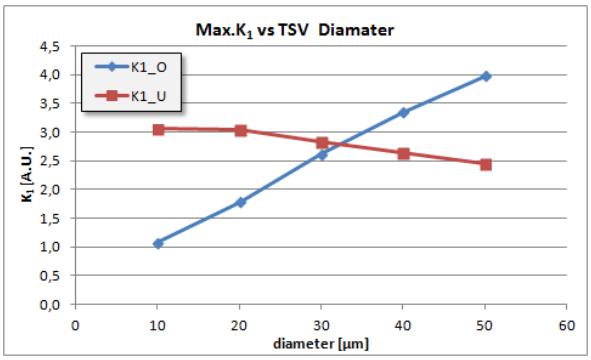



Fig. 9 $K_1$-progress of both initial material interface crack vs. TSV diameter

While $K_1$ moderate decreases at the lower interface it increases remarkable with greater TSV diameter. Simultaneously $K_2$ increases with the TSV diameter with phase angles between 70° and 89°. In summary, we have dominating shear mode situations at these interfaces for both, changing thickness of the Nickel layer and changing TSV diameter.

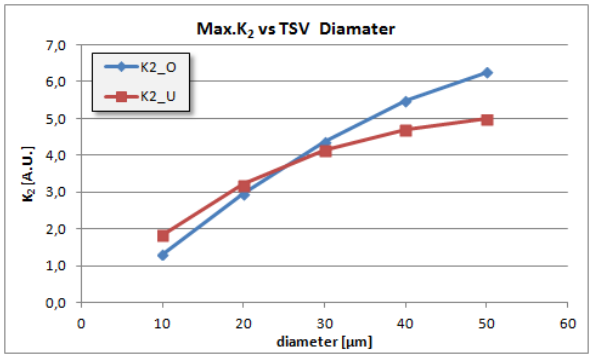



Fig. 10 $K_2$-progress of both initial material interface cracks vs. TSV diameter

Furthermore, TSV with smaller diameter show lower delamination risks at the examined interfaces. Statements in view of Nickel layer thickness dependence on delamination risks are not possible at the moment because of missing fracture toughness properties – especially their dependence on the phase angle.

## 4. Crack Initiation and Propagation in Silicon

It is widely discussed in the literature that copper-TSV causes pumping and protrusion perpendicular to the upper and lower surface as a result of the CTE mismatch between copper and silicon. But, at the same time the expanding or shrinking copper causes pressure or tension in the surrounding silicon. Since this is also the case at room temperature (because of the residual stresses) measurements by means of Raman spectroscopy show increased stress levels close to the TSVs – see also [6].

On the other hand, there is probably a cracking risk within the silicon die that has to be evaluated. For this purpose an X-FEM approach was utilized to discuss crack initiation and propagation under different loading conditions. It uses Heaviside enrichment functions – Eq. (3)

$$u^h(x) = \sum_{I \in N} N_I(x) \left[ u_I + H(x) a_I + \sum_{\alpha=1}^{4} F_\alpha(x) b_I^\alpha \right], \quad (3)$$

were H(x) is the Heaviside enrichment term for nodes belonging to elements cut by the crack and $\sum F_\alpha$ stands for the crack tip asymptotic functions for nodes belonging to elements containing a crack tip – see more in detail in [5]. To perform simulations with X-FEM it is necessary to either use classic, linear elastic fracture mechanics – the VCCT approach – or cohesive damage mechanics for crack initiation and propagation description. The latter was used here. That's why, a maximum principal stress level together with mixed mode fracture energy properties and damping viscosity were defined for the traction separation law and damage stabilization. The X-FEM simulations assuming initial cracks at 2 different locations and 2 different initial stress levels show the crack paths as results – see Fig. 11 to Fig. 14. The model consists of 2 neighboring TSVs and symmetry boundary conditions left plus periodic boundary conditions right. The pitch is set to 71 µm and the TSV-diameter is taken as 20 µm. The whole silicon region is prepared for use as X-FEM enrichment region. The copper-TSV and liner/barrier region are suppressed here for better visualization of stress fields and crack paths.

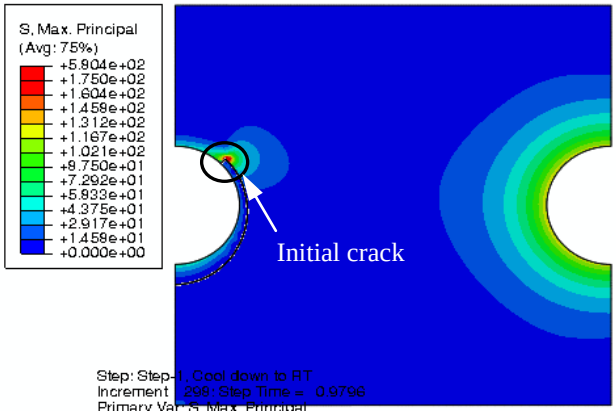



Fig. 11 Initial crack located at the side wall of one TSV; cool down from stress free temperature 160 °C to RT

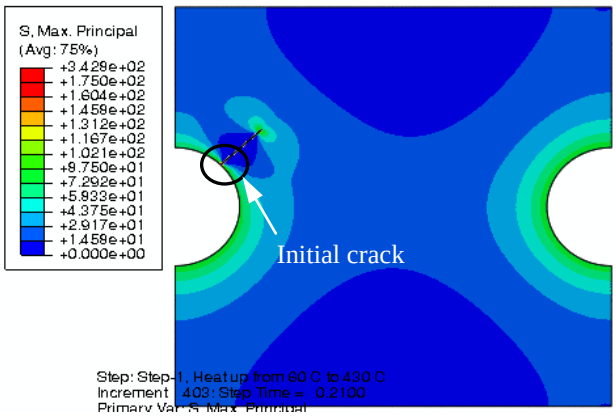



Fig. 12 Initial crack located at the side wall of one TSV; heat up from stress free temperature 60 °C to 430 °C

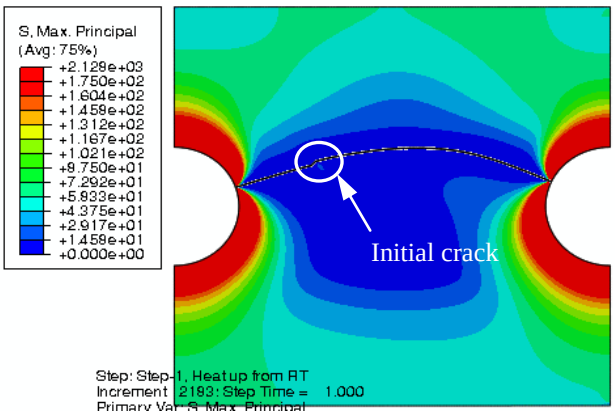



Fig. 13 Initial crack located between the 2 TSVs; heat up from stress free temperature 60 °C to 430 °C

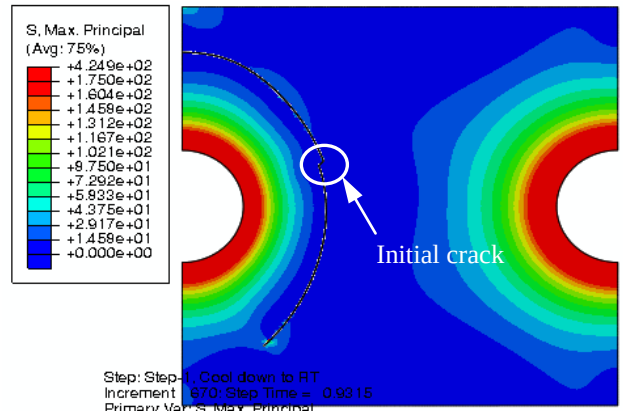



Fig. 14 Initial crack located between the 2 TSVs; cool down from stress free temperature 160 °C to RT

Fracture toughness for mode I cracking and the crack initiation stress level had to be reduced in order to force cracking. Looking at the results a bit closer indicates clearly:

1. Heating up from a lower stress free temperature results in pressure within the TSV and tensile stresses in silicon perpendicular to the x-axis → the crack opens and propagates into silicon towards the next high tensile stress region (the next TSV) – see Fig. 12 and Fig. 13. In case of Fig. 12 the crack propagation speeds up to catastrophic level after a short way.
2. Cooling down from a higher stress free temperature to RT results in tension within the TSV and tensile stresses perpendicular to the TSV side wall → the crack kinks immediately and surrounds the nearest located TSV independent of its origin – see Fig. 11 and Fig. 14. Delamination at the copper-barrier interface is also imaginable, of course.

These crack paths look as expected from engineers understanding. Consequently, the crack paths found this way could also help to identify the thermo-mechanics behind an observed failure pattern in the future.

## 5. Conclusions

Thermal copper-TSVs as an important component of 3D-integration provide an elegant solution to effectively transfer heat from LED to the heat spreading structures on the backside of a substrate or die. But, the use of copper-TSVs generates also novel challenges for reliability analysis and prediction, i.e. to manage multiple failure modes - interface delamination, cracking and fatigue, in particular. Therefore, the authors show results of simulative work to overcome cracking and delamination risks in the vicinity of thermal copper-TSVs by means of fracture mechanics approaches. An interaction integral approach is utilized within a simulative DoE and X-FEM is used to help clarifying crack propagation paths in silicon. Methodology and results provided a good insight into the role of model parameters for further optimizations of the intended thermal TSV-approaches in LED packaging applications and could also help to identify the thermo-mechanics behind observed failure patterns in further applications.

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