On the Application of Advanced Crack Initiation and Propagation Evaluation Techniques in Micro- and Nanotechnologies

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Abstract
3D-integration becomes more and more an important issue for advanced LED packaging solutions as it is a great challenge for the thermo-mechanical reliability to remove heat from LEDs to the environment by heat spreading or specialized cooling technologies. Thermal copper-TSVs provide an elegant solution to effectively transfer heat from LED to the heat spreading structures on the backside of a substrate. But, the use of copper-TSVs generates also novel challenges for reliability as well as also for reliability analysis and prediction, i.e. to manage multiple failure modes acting combined - interface delamination, cracking and fatigue, in particular. In this case, the thermal expansion mismatch between copper and silicon yields to risky stress situations. Therefore, extensive simulative work was performed to overcome cracking and delamination risks in the vicinity of copper-TSVs by means of fracture mechanics approaches. Especially, an interaction integral approach is utilized within a simulative DoE and X-FEM is used to help clarifying crack propagation paths in silicon. The DoE-based response surface methodology provided a good insight into the role of model parameters for further optimizations of the intended thermal TSV-approaches in LED packaging applications.

Key words: 3D-integration, TSV, fracture mechanics, interaction integral, X-FEM

1. Introduction

The 3D IC-integration using through-silicon-vias (TSV) has gained remarkable momentum for industry adoption. It speeds up for further miniaturization, higher performance, lower power consumption and heterogeneous integration. That offers great advantages for the interconnect bandwidth, reduced wire delay, increase of packaging density together with heterogeneous chips. World-wide, several full 3D process flows have been established. However, 3D IC-integration comes with the implementation of many new processes and materials that may affect behaviour and reliability of the overall system. So, TSVs in 3D IC may cause significant thermal mechanical stresses, which not only result in systematic mobility/performance variations, but also lead to mechanical reliability concerns such as fatigue failure, cracking, and interfacial delamination, in particular. This is not only of interest for the reliability of completed assembly but, already during the various steps of manufacturing (BEoL stack build up for instance) and assembling (reflow soldering etc.).

Thus, very detailed local effect modeling together with full-chip/package, multi-scale modelling and physical design tools need to be developed to achieve more reliable 3D IC-integration technologies

[1-2]. In addition, several experimental methods need to be utilized to verify the simulations results and to deliver material parameters (nano-Indentation), residual stresses from manufacturing (fibDAC – determines stress released by Focused Ion Beam milling by means of digital image correlation algorithms) and changes of the material morphology (Electron Backscattering Diffraction).

As a result of the ongoing progress in the development of smart lighting applications 3D-integration becomes also an important issue - advanced LED packaging solutions, in particular. To remove heat from LEDs to the environment by heat spreading or specialized cooling technologies is a great challenge for the thermo-mechanical reliability in this context. Thermal copper-TSVs provide an elegant solution to effectively transfer heat from LED to the heat spreading structures on the backside of a substrate. But, the use of copper-TSVs generates also novel challenges for reliability as well as for reliability analysis and prediction, i.e. to manage multiple failure modes acting combined - interface delamination, cracking and fatigue. In this case, the huge thermal expansion mismatch between copper and silicon yields to risky stress situations. Furthermore, out of plane pumping and protrusion of copper is a challenge for the metal- and dielectric layers covering the TSV during manufacturing (reflow soldering) and also during passive and active thermal cycling tests. First investigations demonstrate that these effects depend highly on the temperature dependent elastic-plastic behaviour of TSV-copper and the residual stresses determined by the electro deposition chemistry as well as on the annealing conditions.

Therefore, a combined simulative/experimental methodology is used to overcome cracking and delamination risks in the vicinity of the thermal copper-TSVs by means of fracture mechanics approaches. Especially, an interaction integral approach is utilized within a simulative DoE and X-FEM is used to help clarifying crack propagation paths in silicon. The DoE-based response surface methodology provided a good insight into the role of model parameters for further optimizations of the intended thermal TSV-approaches in LED packaging applications – see figure 1.

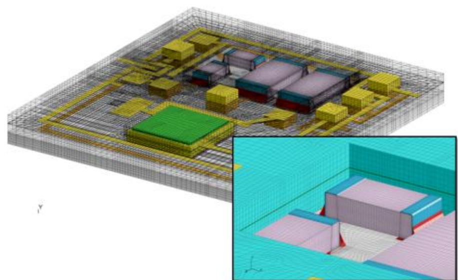

Figure 1: 2D/3D Wafer Level integration of a power module

2. Delamination Risk near TSV

Apart from thermal management point of view thermo-mechanical issues have to be taken into account - the handling of the package in particular. For example, the thermo-mechanical loading of the silicon-carrier during the solder reflow and cooling down is of great interest in view of delaminations and damaging of metal and dielectric layers adjacent to the copper-TSV. Figure 2 shows details of the TSV-vicinity of the simulation model. Especially the material interfaces near the TSV – marked by ellipses – between copper and the thin SiO_2-layer as well as between copper and nickel seem to be sensitive to delamination. The nonlinear FE-model is fully parameterized taking temperature dependent elastic-plastic as well as creep behaviour of materials into account – see figure 2. Moreover, possible contact of

the crack flanks is considered, as well.

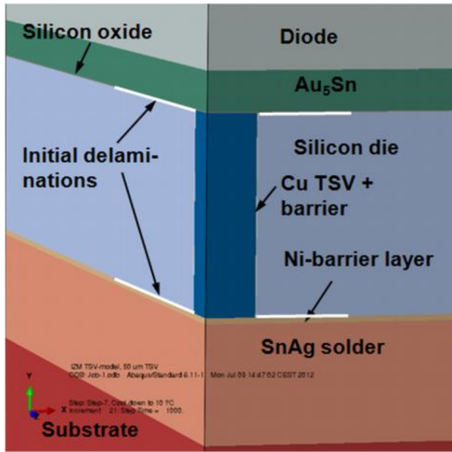

Figure 2: Detail of the design of the LED-Package in the surrounding of a Copper-TSV

The investigation of the delamination risk during the thermal handling is performed with the J-integral as implemented in the commercial FE-code ABAQUS [3].

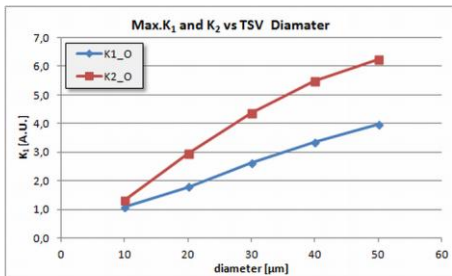

Figure 3: Progress of stress intensity factors of upper initial delamination vs. TSV diameter

One question to answer within the extensive simulative DoE is related to the influence of the TSV diameter: follow or not the rules found by thermal simulations: multiple tiny TSVs show better thermal performance. Figure 3 show clearly that TSV with smaller diameter show lower delamination risks at the examined interface.

3. X-FEM Simulates Crack Initiation and Propagation in Silicon

Copper-TSV pumping and protrusion perpendicular to the upper and lower surface as a result of the CTE mismatch between copper and silicon are widely discussed in the literature. But, at the same time the expanding or shrinking copper causes pressure or tension in the surrounding silicon.
Therefore, there is probably a cracking risk within the silicon die that has to be evaluated. For this purpose an X-FEM approach was utilized to discuss crack initiation and propagation under different loading conditions.
The X-FEM simulations assuming initial cracks at 2 different locations and 2 different initial stress levels show the crack paths as results. The model consists of 2 neighbouring TSVs and symmetry boundary conditions left plus periodic boundary conditions right. The whole silicon region is prepared for use as X-FEM enrichment region. The copper-TSV and liner/barrier region are suppressed here for better visualization of stress fields and crack paths.

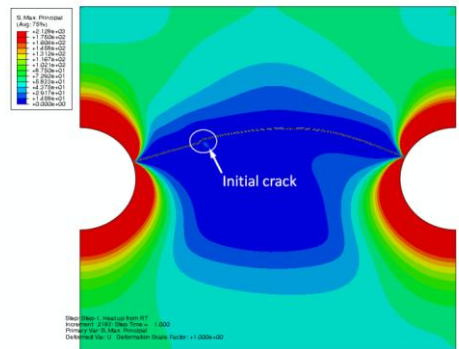

Figure 4: Initial crack located between the 2 TSVs; heat up from stress free temperature 60 °C to 430 °C

Fracture toughness for mode I cracking and the crack initiation stress level had to

be reduced in order to force cracking – see results in [4]. Looking at the results a bit closer indicates clearly:

1. Heating up from a lower stress free temperature results in pressure within the TSV and tensile stresses in silicon perpendicular to the x-axis: the crack opens and propagates into silicon towards the next high tensile stress region (the next TSV) – see figure 4.
2. Cooling down from a higher stress free temperature to RT results in tension within the TSV and tensile stresses perpendicular to the TSV side wall: the crack kinks immediately and surrounds the nearest located TSV independent of its origin.

These crack paths look as expected from engineers understanding. Consequently, the crack paths found this way could also help to identify the thermo-mechanics behind an observed failure pattern in the future.

4. Conclusions

Thermal copper-TSVs as an important component of 3D-integration provide an elegant solution to effectively transfer heat from LED to the heat spreading structures on the backside of a substrate or die. But, the use of copper-TSVs generates also novel challenges for reliability analysis and prediction, i.e. to manage multiple failure modes - interface delamination, cracking and fatigue, in particular. Therefore, the authors show results of simulative work to overcome cracking and delamination risks in the vicinity of thermal copper-TSVs by means of fracture mechanics approaches. An interaction integral approach is utilized within a simulative DoE and X-FEM is used to help clarifying crack propagation paths in silicon. Methodology and results provided a good insight into the role of model parameters for further optimizations of the intended thermal TSV-approaches in LED packaging applications and could also help to identify the thermo-mechanics behind observed failure patterns in further applications.

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