A Comparison of Receiver Topologies for Digital Load-Side Transmission in General LED Lighting

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***Abstract*—Digital Load-Side Transmission (DLT) is a two-wire bound power line communication methodology that has been specifically developed for general lighting applications and transmits data over mains. This paper proposes three DLT receiver concepts and compares them to one other regarding robustness, complexity and power consumption. All of these detectors have been realized and tested in hardware. To evaluate robustness in terms of utility grid variations, 24-hour long term measurements have been taken for each concept, when connected to 50 Hz mains. A telegram error rate (TER) has been measured for all setups, while the power consumption of the implemented receivers has been determined by Simulation Program with Integrated Circuit Emphasis (SPICE) simulations. A fully digital approach and an active analog bandpass based structure seem to be the most promising solutions as they feature comparable TERs of 44 and 80 parts per million (ppm), respectively. All presented topologies can be monolithically integrated on a chip to facilitate development of highly integrated, intelligent LED drivers.**

I. Introduction

Light emitting diodes (LED) have been introduced into general lighting applications due to several benefits in contrast to conventional light sources, such as high efficiency, long lifetime and the absence of toxic compounds [1]–[3]. In fact, LEDs are about to become the predominating illumination device in homes and offices. Further significant power savings can be achieved on a system level, if a certain level of intelligence is applied to the luminaires. Intensity, location and time of illumination can hence be controlled precisely [4] and offer in conjunction with sensor nodes the ability to operate automatically or react on predefined events, such as presence detection or breaking dawn.

In order to enable such smart functionality, the LED based luminaires have to be equipped with a communication unit. In literature, different approaches from wireless solutions like Zigbee or Bluetooth up to modern power line communication (PLC) methods, such as Orthogonal Frequency-Division Multiplexing (OFDM) [5], [6] or P-BUS [7], have been proposed to overcome that issue. Wireless communication techniques are usually more complex than PLC systems [7] and thus might require additional hardware effort. High data rate approaches for power line communication using OFDM suffer from interference caused by LED luminaire power supplies [8] and might require circuitry of relatively high complexity. Since a low data rate is sufficient for controlling an intelligent luminare, a low frequency approach is beneficial for LED lighting applications. In addition, LED power supplies emit less noise on lower frequencies [8]. A suitable approach is the P-BUS system [7], which is yet limited to operate on low voltage direct current (DC) power only.

Since luminaires have to be attached to mains anyway, it is favorable to utilize a PLC technology that transmits data over the alternating current (AC) grid voltage as no additional wiring would be required in that case. Hence, a novel PLC technology called *'Digital Load-Side Transmission'* (DLT) has been specifically developed for general lighting applications in homes and small offices and is about to be standardized [9]. A functional block diagram of an intelligent LED lighting system with DLT communication is depicted in Fig. 1. More information about the DLT methodology is provided in the next section.

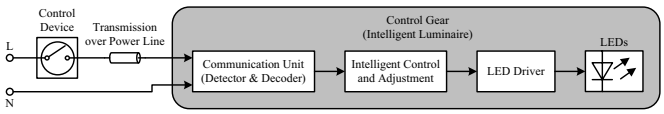

Fig. 1. System Concept of an intelligent luminaire embedded in a DLT communication structure.

In this paper, mains or grid voltage refers to the European utility grid using a root mean square (rms) voltage of 230 V and a frequency of 50 Hz. Thus, all receivers have been designed for these specifications. However, adoption of the developed detectors to other utility grids is possible with minor changes. In total, three different receiver topologies for DLT communication systems are presented in this work. Section II provides the relevant information on DLT for designing an appropriate receiver. Subsequently, the three different receiver topologies are presented in section III, while section IV comprises measurement data and performance evaluation. Finally, section V concludes this work and sums up the relevant results.

II. Power Line Communications with DLT

DLT is a unidirectional, low data rate power line communication methodology operating directly on AC mains and is specialized for general lighting applications. A DLT *'control device'* replaces a conventional phase-cut dimmer or a light switch. To maintain compatibility with existing installations, it has to be connected in series with one or more parallel connected intelligent luminaires (*'control gears'*). DLT encodes two information bits per half-wave and therefore transmits control commands in a telegram structure over several half-waves

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of mains. Since DLT is a two-wire communication system, it is a very simple and robust technology that is also compatible to existing wiring, which may not feature a neutral wire at the switch connection port. Furthermore, DLT does not require any band elimination filter as it just influences the supply line between the control device and the control gears. Hence, it is possible to operate multiple DLT control devices, each with its own control gears, on a single phase without interference. Additionally, DLT is compatible to conventional light sources like compact fluorescent lamps (CFL) and incandescent lamps. Therefore, it has several distinct advantages over most other PLC systems.

The upcoming DLT standard [9] divides every half-wave of the grid voltage into three periods, namely a supply period, an operating period, and a data period. The supply period can be further divided into three phases, which are one high current (HC) surrounded by two low current (LC) intervals. Fig. 2 illustrates the described classification by means of a measured voltage signal of one half-wave supplied to a DLT control gear. The supply period is used to power the control device while the operating period supplies the control gear. During the data period information is passed from the control device to the control gear. As indicated in Fig. 2, the crossover from supply to operating period and from operating to data period happens at the predetermined voltage V_{SW}.

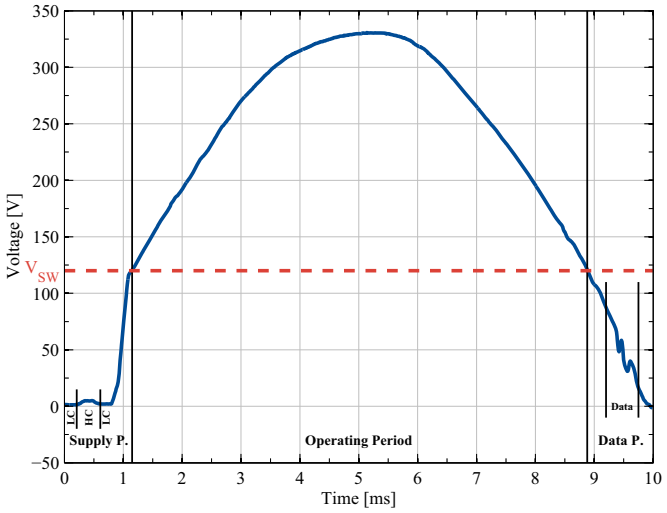


Fig. 2. DLT voltage waveform measured at the input of a *'control gear'*.

For designing a suitable DLT receiver, two main aspects have to be considered as pointed out in the following. First, the intelligent luminaire needs to have a bypass structure in order to provide the required high and low current flows during the supply and data periods. Second, the definitions of data encoding within the data period and telegram structure have to be known for proper decoding. Every half-wave contains a so-called data frame, which can be subdivided into six *'half-bits'* as follows: One start-of-frame (SoF) half-bit, two Manchester-coded information bits (four half-bits) and one stop half-bit. Fig. 3 illustrates the correlation of timing and voltage of the modulated data, where t_{HB} specifies the duration of one half-bit and V_{data} the modulation depth. Referring to a single frame the decoder has to distinguish five different cases. The Manchester coded information bits with their corresponding half-bit sequences are listed in Table I.

As mentioned above, a complete DLT command, e.g. brightness, is transmitted over several half-waves in a telegram structure. A telegram consists of the following sections:

- Start-of-telegram (SoT) frame (first 5 half-bits high)
- Group number (2 information bits)
- Telegram type (3 information bits)
- Parity (1 information bit)
- Payload data (length depends on telegram type)

Fig. 4 exemplarily illustrates a complete brightness telegram sent over eight consecutive half-waves.

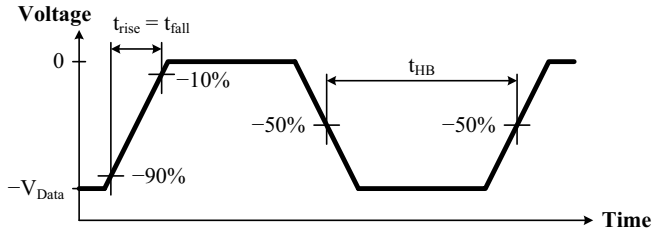


Fig. 3. Specification of physical data transmission.

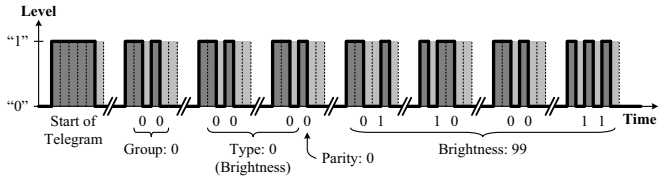


Fig. 4. Example of a single brightness telegram.

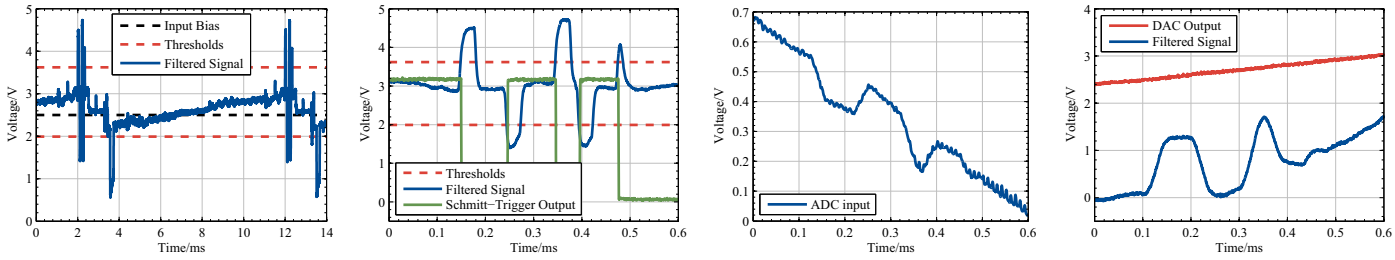
TABLE I. MANCHESTER CODED HALF-BIT SEQUENCES AND ENCODED INFORMATION BITS

Case #	Half-bit sequence	1^{st} info bit	2^{nd} info bit
1	{1 1 0 1 0 0}	0	0
2	{1 1 0 0 1 0}	0	1
3	{1 0 1 1 0 0}	1	0
4	{1 0 1 0 1 0}	1	1
5	{1 1 1 1 1 0}	SoT	SoT

III. DLT RECEIVER CONCEPTS AND IMPLEMENTATION

The ultimate design goal is to find a DLT receiver solution that can be integrated on a chip because that would enable intelligent and efficient LED drivers with a small form factor. Therefore, this work can be seen as a pre-study for a later integration to find the most promising receiver approach. However, the demand of integration feasibility puts special restrictions on the detector design as sizes and values of utilized components are limited.

Since the detector has to record the DLT data from every half-wave of the grid voltage, the rectified mains frequency of 100 Hz is present in the signal spectrum. However, the DLT data signal frequency is just one to two decades higher than that, depending on the transmitted data. Therefore, a typical bandpass filtering of the complete DLT signal, which might have been the most obvious solution, comes along with two main problems. At first, a bandpass structure with high attenuation is required to suppress the influences originating



(a) Detector #1, $C_2 = 49\,\text{pF}$ (b) Detector #1, $C_2 = 49\,\text{pF}$ (c) Detector #2 (d) Detector #3

Fig. 5. Measurements of filter signals for the different receiver topologies.

from the grid frequency, but a higher order bandpass would increase design complexity. Second, and even more restrictive, the component values of capacitors and resistors would be relatively high. Therefore, an approach employing a band pass filter with a center frequency of about 10 kHz becomes impractical for an integrated solution. Considering the finite slew rate of the modulated data, a better solution can be found. Obviously, the edges in the data signal comprise higher frequency components. Thus, building an edge detector would lead to a higher center frequency of the bandpass filter and hence smaller component values. Within this work three different DLT receiver topologies have been developed as shown in the following. All of these concepts rely on edge detection.

A. *Detector #1: Active Bandpass with Schmitt-Trigger*

The first DLT detector concept consists of a typical active bandpass structure, which can here be seen as a differentiator, in conjunction with a Schmitt-Trigger. Fig. 6 illustrates the proposed filter structure.

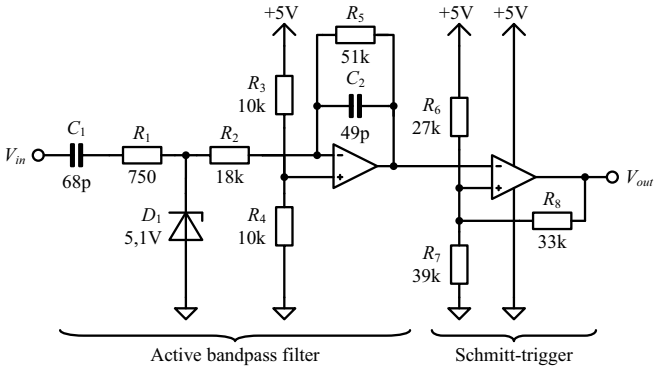


Fig. 6. Schematics of detector #1: Active bandpass with Schmitt-Trigger.

Reducing the capacitance of capacitor C_2 enables tuning of the effective center frequency of the active bandpass filter and increases its bandwidth, as can be seen from equation 1. In doing so, it has been possible to test and verify two different implementations of this receiver concept. Capacitor values of $C_{2,a} = 49\,\text{pF}$ and $C_{2,b} = 25\,\text{pF}$ have been used resulting in center frequencies of around 88 kHz and 125 kHz, respectively. Fig. 5a and 5b show the filtered signal for $C_2 = 49\,\text{pF}$.

$$H(s) = \frac{-sR_5C_1}{(1 + s(R_1 + R_2)C_1) \cdot (1 + sR_5C_2)} \quad (1)$$

This DLT detector concept is purely analog and straightforward to implement with low complexity, which makes it attractive for an integrated design. However, the received Manchester-coded data bits of a single half-wave need to be decoded and reassembled to a complete telegram in the digital domain. Fortunately, the Schmitt-Trigger operates as a 1 bit analog-to-digital converter (ADC) and hence already performs a signal digitalization. Because the Schmitt-Trigger has furthermore taken care of signal reconstruction, the decoder only needs to evaluate the received frames and reassemble them into complete telegrams. The digital decoding has been fully implemented on a microcontroller for verification purposes.

To decode the received information the decoder simply applies a counter, which measures the time between two adjacent edges. In this way the binary data of each half-bit is easily decoded and can then be stored in a register. The information bit values have to be restored afterwards by a state-machine according to the five independent cases described in section II. Fig. 7 shows the flowchart of the decoder's half-bit evaluation.

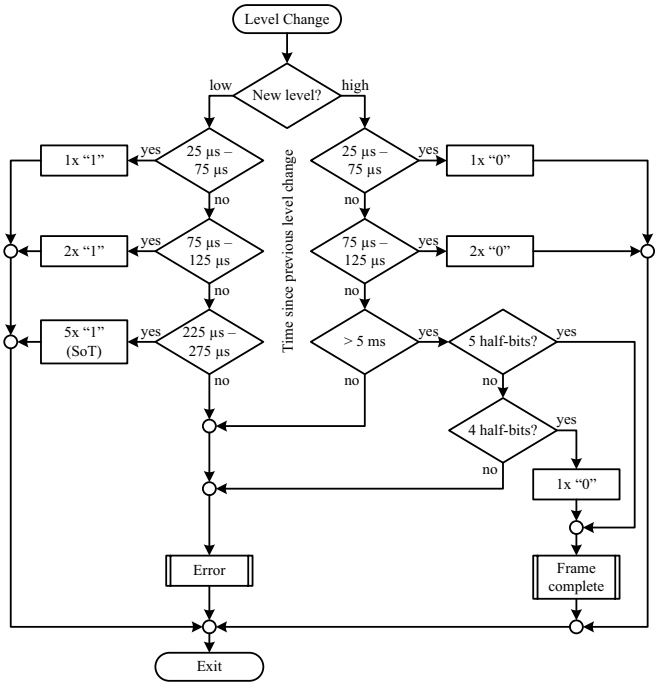


Fig. 7. Flowchart of the implemented DLT frame decoder.

Every time an edge occurs, the routine evaluates the current logic level. Depending on the time difference to the previous edge, the respective half-bit value(s) is (are) saved in a register. For the first positive edge of a frame the decision engine will always follow the right path and check whether a long time (here: 5 ms) has passed, because the last data period has preceded the current one for almost 10 ms. This step is necessary to identify the start of a new frame. After recognizing the start of a new frame, the state machine checks whether four or five half-bits have been recorded in the previously recorded frame. In case of a four half-bit sequence an additional *'zero'* has to be added, because the last half-bit has not generated an edge, as it equals zero. Subsequently, the evaluation subroutine is called, which converts the half-bit sequences to information bits according to Table I and then performs the telegram evaluation. The flowchart for this telegram reconstruction and evaluation is illustrated in Fig. 8 for the three most relevant telegrams.

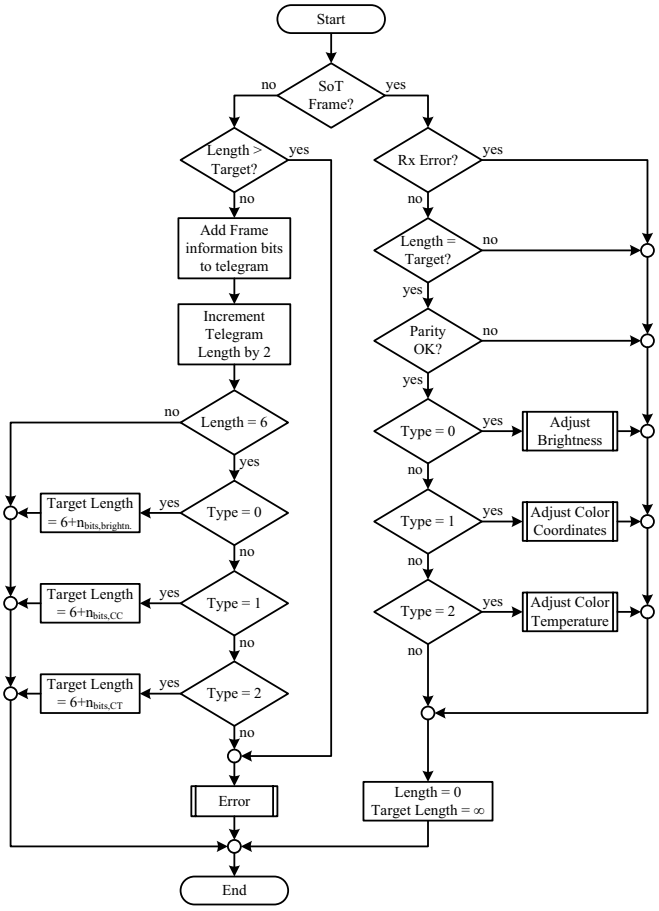


Fig. 8. Flowchart of the DLT telegram reconstruction and evaluation for the most common telegram types.

At first, it is checked whether the frame indicates the start of a new telegram. This step is performed for synchronization. Once a SoT-frame has been received, the previously recorded telegram is evaluated. In case no telegram has been detected yet (start-up), the examination of actual and target telegram length will yield a *'no'* because the actual telegram length is initially set to zero and the target length is initialized to be infinite. When receiving regular data frames, the decoder will follow the left-hand part of the flowchart. Within this path the two information bits of the current frame are added to the current telegram, unless the telegram length has exceeded its target limit. Afterwards the telegram length is increased by two. When a length of six is reached, the telegram type can already be determined. The target length for the current telegram is now set corresponding to the telegram type. The following information bits represent the payload data of the telegram and are simply added to the current telegram. When the next SoT-frame occurs, the previously received telegram is evaluated. The described algorithm has also been implemented on the microcontroller.

It can be seen that error detection has been introduced on half-bit, frame and telegram level. Telegram length and parity bit represent a further security mechanism to prevent from decoding false signals. If an error is detected within any of these levels, the entire telegram is ignored. Hence, determining a bit error rate (BER) is not only difficult, but simply not feasible due to the DLT structure. However, a quantitative statement about a *'telegram error rate'* (TER) can be made instead. This measure is important for evaluating robustness of the different receiver topologies as explained later.

B. Detector #2: Resistive Divider with Digital Filtering

The second detector concept divides the amplitude of the grid voltage down into the 3.3 V domain of the microcontroller performing the analog to digital conversion by an 11 bit ADC. A measurement of the ADC input voltage is depicted in Fig. 5c. The ripple is caused by the ADC sampling on the high-impedance signal. The sampled waveform is subsequently passed through the digital filter as depicted in Fig. 9.

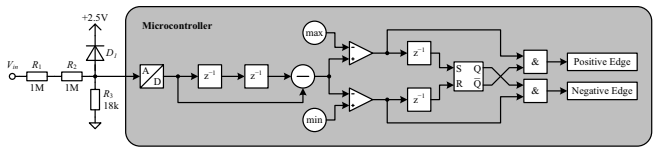


Fig. 9. Schematics of detector #2: Resistive Divider with Digital FIR Filter.

The delay elements form in conjunction with the sampled input signal and the subtraction element a third order finite impulse response (FIR) filter that acts as a differentiator. The resulting signal is fed into a window comparator, which detects rising and falling edges and passes the corresponding logical levels to the AND gates and delayed by one clock cycle to the flipflop inputs. The SR-flipflop and the AND gates prevent the detection of consecutive edges of the same polarity. Determining the time between two detected edges allows for measuring the time of logical 'low' and 'high' periods of the data signal. In this way the transmitted information bit can be evaluated similar to the software procedure applied to the active bandpass filter illustrated in Fig. 7. Although the flowchart would look slightly different, it is not presented here due to lack of space. The telegram evaluation procedure shown in Fig. 8 is applied for this filter without modification.

This second receiver architecture is slightly more complex compared to the first one because the effort of implementing an on-chip ADC is assumed higher than the design of operational amplifiers. Still, the overall complexity is evaluated to a medium level.

C. Detector #3: Differential Analog Subtraction Filter

The third receiver concept follows the idea of a subtraction in the analog domain in order to directly generate the desired data signal at its output. Fig. 10 presents the circuit implementation. At the negative opamp input, the DLT modulated mains signal and an ideal inverse sinewave are added. This corresponds to a subtraction of an ideal, non-inverted sinewave from mains. Because the two signals should ideally only differ from each other by the modulated DLT data, the lowpass filtered output is expected to deliver the desired data signal directly. Fig. 5d shows an example of this signal, which is then converted into the digital domain. The digital processing is identical to that of the fully digital approach presented in subsection III-B. The telegram evaluation routine used in the other two concepts is employed in this approach as well. Since an additional digital-to-analog converter (DAC) is required for this concept, the complexity is higher in contrast to the other concepts.

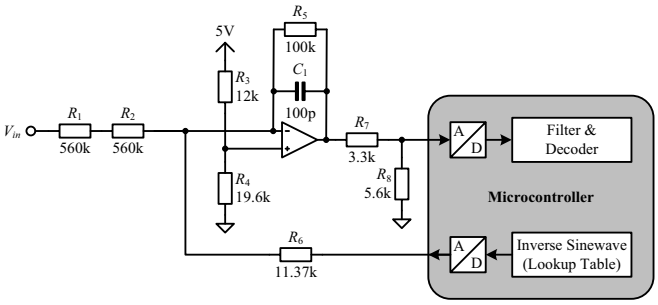


Fig. 10. Schematics of detector #3: Differential analog subtraction filter.

IV. Measurements and Performance Evaluation

All receiver architectures have been implemented in hardware with a microcontroller used for digital signal processing, decoding and evaluation. A photo of the test board is shown in Fig. 11. The microcontroller cannot be seen here because it is situated on a second board.

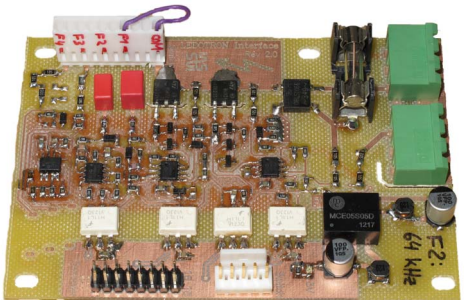


Fig. 11. Photo of the test board including all proposed DLT detector concepts.

The comparison of the different receiver architectures mainly focuses on robustness, complexity and power consumption, while considering a later on-chip integration. Therefore, the mentioned aspects have to be reasonably balanced for a suitable trade-off. Circuit complexity of the three topologies has already been compared in section III. Power consumption and robustness are described more detailed in the following.

A. Power Consumption

The power consumption could only be evaluated by means of SPICE simulations as it was not possible to physically measure the overall current consumption. For each concept the power consumption of the voltage dividers, opamps and reference voltages including power drawn from mains have been included in the computations. Table II sums up these simulation results. However, the power consumption of the microcontroller is not included in this calculation, which results in a distinct advantage for the digital approaches. To fairly compare all topologies to each other regarding power consumption, a rough estimation for a solution on an application specific integrated circuit (ASIC) is provided as well. For a complete DLT receiver, the power consumption of the bypass circuits and zero crossing detector also has to be taken into account. This power consumption is independent of the chosen detector concept and can hence be neglected for the comparison.

TABLE II. Power consumption of proposed DLT receivers.

	Detector #1	Detector #2	Detector #3
SPICE Simulation	37.72 mW	25.73 mW	64.59 mW
Expected for ASIC	$\leq$ 6.5 mW	$\leq$ 7.2 mW	$\leq$ 10.5 mW

It is clearly noticeable that the simulated power consumption of all receivers appears relatively high. This is due to several reasons: The usage of discrete, non-optimized opamps, the usage of resistive dividers for bias voltages and a non-optimized control, i.e. the detectors could be partly switched off in the DLT operating and supply periods. For the ASIC estimation the following assumptions have been made: The power consumption of the integrated opamps was assumed to equal 2 mW maximum, which is a fairly worst-case approximation for these kinds of amplifiers. The resistive divider for the second detector concept has been dimensioned to $(R_1 + R_2) = 20\,\mathrm{M\Omega}$ and $R_3 = 270\,\mathrm{k\Omega}$ leading to a power dissipation of approximately 2.6 mW considering a full-scale deflection of 1.8 V at 135 V input voltage. The power consumption of ADC and DAC can be estimated by equation 2 under the assumption of a total input capacitance of $C_{ADC,in} = 8\,\mathrm{pF}$, a sampling frequency of $f_s = 100\,\mathrm{kHz}$ and digital supply voltage of $V_{DD,dig} = 1.8\,\mathrm{V}$. For all concepts an additional safety margin of around 2 mW is considered in the computation.

$$P_{ADC} = f_s \cdot C_{ADC,in} \cdot V_{DD,dig}^2 = 100\,\mathrm{kHz} \cdot 8\,\mathrm{pF} \cdot (1.8\,\mathrm{V})^2 \approx 2.6\,\mathrm{mW} \quad (2)$$

Obviously, the third detector architecture performs worse in both cases, whereas detector concepts #1 and #2 are comparable regarding power consumption. The main contributor to the power consumption of concept #3 originates from the relatively low impedance of its mains fed input. An input impedance of $R_1 + R_2 = 20\,\mathrm{M\Omega}$, as used for the estimation of the fully digital approach, would be possible but leads to a high value for R_5. This would require a prohibitively large area in an ASIC solution and results in increased costs. Therefore, the third DLT receiver topology is disadvantageous and should only be considered for implementation, if its performance with respect to the TER is significantly better than that of the

other two approaches. Still, a final conclusion can only be drawn after a complete evaluation of receiver robustness and reliability.

B. Robustness

To evaluate the robustness of the receiver topologies, a 24-hour long term measurement has been taken for each concept while connected to regular 50 Hz mains. Hence, the DLT detectors were tested under real operational conditions and exposed to typical distortions on the European utility grid. The amount of faulty as well as correctly decoded telegrams was recorded for the entire measurement time. In this way, a telegram error rate, as mentioned above, can be determined for every receiver approach. Table III gives an overview of the amount of recorded and faulty telegrams for all detectors. The corresponding error rates have been calculated. The peak error rate per minute was below 0.55 % for detectors #1 and #2 and almost 15 % for detectors #3. This indicates clearly that the concepts #1 and #2 perform significantly better than concept #3.

TABLE III. EVALUATION OF TER IN 24-HOUR MEASUREMENTS.

Detector Concepts	Recorded Telegrams	Detected Errors	TER in ppm
#1 ($C_2 = 49$ pF)	1083037	87	80
#1 ($C_2 = 25$ pF)	1079471	61	57
#2	1131627	50	44
#3	1080507	1556	1440

In a second test setup the DLT control device and the receivers under test were connected in series to a synthesized AC voltage. By changing the frequency, reactions to grid frequency variations can be observed. The results are listed in Table IV. Although the allowable frequency variations seems quite limited for detector concepts #2 and #3, these approaches could also be used for different utility grids, such as the one in the United States of America (USA) running at 60 Hz, by adapting the digital filtering correspondingly. All concepts show reasonable results for this test case and are hence well suited for the desired application.

V. CONCLUSION

Three different receiver topologies for a novel power line communication methodology called *'Digital Load-Side Transmission'* (DLT) have been proposed in this work. All detector concepts have been implemented in hardware and a comprehensive comparison regarding complexity, power consumption and robustness has been conducted. Special restrictions have been made on the topologies as they are meant for being integrated on chip. The comparison has further been confirmed with measurement results. Table IV sums up all relevant results of the performed DLT receiver comparison. It can be seen that detector topologies #1 and #2 surpass the third approach in all tested categories. Hence, these two receiver concepts are evaluated to be suitable for an integrated DLT receiver solution. As both concepts show comparable performance in all fields under test, the decision should depend on the best suited integrated circuit (IC) technology for the application. If the digital detector can be used for additional functionality, such as zero crossing detection or generation of the DLT timings for high- and low-current supply phases, the slightly higher power consumption and complexity might be justified. On the other hand, some IC technologies are purely analog. In conclusion, the first two concepts have proven functional with very good performance and robustness and are both suited for highly integrated, intelligent LED drivers.

TABLE IV. COMPARISON OF PROPOSED DLT RECEIVER TOPOLOGIES.

	Detector #1	Detector #2	Detector #3
Circuit Complexity	Low	Medium	High
Telegram Error Rate	87 ppm	44 ppm	1440 ppm
f_{grid} Input Range	40-60 Hz	49.1-50.4 Hz	49.5-50.4 Hz
SPICE Simulation	37.72 mW	25.73 mW	64.59 mW
Expected for ASIC	$\leq$ 6.5 mW	$\leq$ 7.2 mW	$\leq$ 10.5 mW

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